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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 09/891,906  | 06/26/2001  | Robert J. Probsting  | 5646-54             | 1428             |
| 20792   | 7590        | 06/19/2003           | EXAMINER            |                  |
| MYERS BIGEL SIBLEY & SAJOVEC<br>PO BOX 37428<br>RALEIGH, NC 27627 |             |                      | NGUYEN, DANNY       |                  |
|   |             | ART UNIT             | PAPER NUMBER        |                  |
|   |             | 2836                 |                     |                  |

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                 |                       |
|------------------------------|-----------------|-----------------------|
| <b>Office Action Summary</b> | Application No. | Applicant(s)          |
|                              | 09/891,906      | PROEBSTING, ROBERT J. |
|                              | Examiner        | Art Unit              |
|                              | Danny Nguyen    | 2836                  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 26 June 2001.

2a) This action is **FINAL**.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1,2,4-7,13,14 and 16-22 is/are rejected.

7) Claim(s) 3,8-12 and 15 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.

4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Specification***

1. The disclosure is objected to because of the following informalities: the US provisional application series Number is missing. Appropriate correction is required.

### ***Oath/Declaration***

2. The oath or declaration is defective because the oath/declaration is missing the provisional claim priority form. The New oath/declaration is required.

### ***Claim Objections***

3. Claim 4 is objected to because of the following informalities: Page 15, line 7, the phase "voltage at a gate of pass transistor" should be read "voltage at the gate of pass transistor". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4-7, 13, 14, 16-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Okumura (USPN 5,541,546).

Regarding to claim 1, Okumura discloses an over-voltage protection circuit comprises a pass transistor (107) having a first and a second current carrying terminals (the source and the drain of the pass transistor 107) electrically connected to an input (input terminal I) and an output signal line (the output O, see fig 1) respectively, a voltage clamping circuit (100) comprising first and second diodes (such as 302 and 303 shown in fig. 4) connected in series between a power supply line (Vc) and a gate of the pass transistor (the gate of the pass transistor 107).

Regarding to claim 2, Okumura discloses the first and second diodes comprise first and second NMOS transistors (302 and 303 shown in fig 4) respectively.

Regarding to claims 4, 5, Okumura discloses an over-voltage protection circuit (fig. 1 and 4) comprises a pass transistor (107) having a first and a second current carrying terminals (the source and the drain of the pass transistor 107) electrically connected to an input (input terminal I) and an output signal line (the output O, see fig 1) respectively, a voltage clamping circuit (100, shown in fig. 4) that is electrically connected to a power supply line (Vc) and a gate of the pass transistor (107) and dynamically clamps a capacitively bootstrapped voltage at the gate of the pass transistor (107) within a first range (such as Vc must be lower than 3.2 volts) so that the magnitudes of voltages across the pass transistor (107) do not exceed a voltage in excess of about Vdd (such as 3Volts) when Vin (internal supply voltage 5 volts) is equal to about 2Vdd, where Vin equals a voltage of an input supply and Vdd equals a power supply voltage on the power supply line (Vc)(col. 9, lines 45-47).

Regarding to claim 6, Okumura discloses the voltage clamping circuit (100) comprises an NMOS transistor (such as 302) that is connected as a diode between a power supply line (Vc) and the gate of the pass transistor (107), and wherein a maximum voltage within the first range is equal to about Vdd plus Vth (col. 9, lines 45-47).

Regarding to claim 7, Okumura discloses the voltage clamping circuit (100) comprises first and second diodes (such as 302 and 303) electrically connected in series between the power supply and the gate of the pass transistor (107).

Regarding to claims 13, 19, Okumura discloses an over-voltage protection circuit (fig. 1 and 4) comprises first and second pass transistor (101 and 107) electrically connected in parallel between an input terminal (input terminal I) and an output terminal (the output terminal O), a first power supply line (V2) electrically coupled to a gate of the second pass transistor (101), a second power supply line (Vc), a voltage clamping circuit (100 shown in fig. 4) comprising first and second diodes (such as 302 and 303) electrically connected in series between the second power supply (Vc) and a gate of the first pass transistor (107).

Regarding to claims 14, 18, Okumura discloses the first and second diodes comprises first and second NMOS transistors (302 and 303 shown in fig 4) respectively.

Regarding to claims 16, 17, Okumura discloses the voltage clamping circuit (100) clamps the gate of the first pass transistor (107) at a maximum voltage of about Vdd2 (V1) plus Vth2 in response to a positive input voltage transition in excess of about Vth1

plus  $V_{th2}$  (the thresholds of the pass transistor 101 and 107) and at minimum voltage of about  $V_{dd2}-V_{th1}$  (col. 8, lines 48-60).

Regarding to claims 20, 21, 22, Okumura discloses an over-voltage protection circuit (fig. 1 and 4) comprises a pass transistor (107) having a first and a second current carrying terminals (the source and the drain of the pass transistor 107) electrically connected to an input (input terminal I) and an output signal line (the output O, see fig 1), a voltage clamping circuit (100, shown in fig. 4) that is electrically connected to a gate of the pass transistor (107), clamps a voltage at the gate to a first voltage below a maximum voltage on the input line upon completion of pull-up and clamps the voltage at the gate to a second voltage that is higher than a minimum voltage on the input line upon completion of a pull-down interval (col. 8, lines 48-60).

***Allowable Subject Matter***

5. Claims 3, 8-12, 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 3, 8, and 15 recite an over-voltage protection circuit comprises a voltage clamping circuit having a second NMOS transistor, wherein a source of the second NMOS transistor is electrically connected to a drain and gate of the first NMOS transistor and the power signal line.

The references of record do not teach or suggest the aforementioned limitation, nor would it be obvious to modify those references to include such limitation.

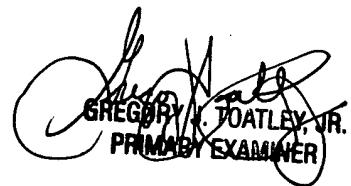
***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (703)-305-5988. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703)-308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-872-9318 for regular communications and (703)-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

DN  
DN  
June 9, 2003



GREGORY V. TOATLEY, JR.  
PRIMARY EXAMINER